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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,643	02/13/2002	Young-Beom Jang	8045-36 (PX1344-US/SSD)	9381

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,643	JANG, YOUNG-BEOM	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 5-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 5-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 05/18/2006.

2. Claims 1 and 5-21 are pending in this application. Claims 1, 7, 10-11, 14, and 17-21 are independent claims. This Office Action is made final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 5-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Pasko et al. ("Optimization Method for Broadband Modem FIR Filter Design using Common Sub-expression Elimination").

Re claim 1, Pasko et al. disclose in Figures 1-3 a filter coefficient design method (abstract) in a digital filter (FIR filter in abstract lines 1-5 page 100) having a plurality of filter coefficients that are expressed with CSD code words of n bits (n: natural number more than 2) (e.g. page 100 right column lines 9-16), comprising the step of: making code word sub-expression for random filter coefficients out of the filter coefficients as a virtual common sub-expression not originally common to any filter coefficients that is relevant to a predetermined common sub-expression so that a plurality of adders are

shared with the predetermined common sub-expression in tap lines of the random filter coefficients (e.g. Figure 2 and left column page 101 under method overview section), wherein the virtual common subexpression has a single bit shifted, added or inverted relative to the predetermined common subexpression (e.g. Figure 1 wherein the code word sub-expression is part b, the predetermined common subexpression is shifted and added part in b, and the virtual common subexpression is the CSE of CSD as seen in c comprising at least a predetermined common subexpression).

Re claim 5, Pasko et al. further disclose in Figures 1-3 the virtual common sub-expression becomes identical to the common sub-expression through at least two more processes out of bit-shift, bit-add and bit-inversion (e.g. Figure 3 contains all the shift, add, subtract/inversion).

Re claim 6, Pasko et al. further disclose in Figures 1-3 the digital filter is a linear phase FIR filter (e.g. Figure 3a).

Re claim 7, Pasko et al. disclose in Figures 2-3 a method for receiving and filtering input signals of digital samples of k bits (k: natural numbers more than 4) in a digital filter having filter characteristics that are created by filter coefficients being expressed as CSD code words of n bits (n: natural numbers more than 2), comprising the steps: creating as a virtual common sub-expression not originally common to any filter coefficients (e.g. CSD coefficients set-optimized in Figure 2) common sub-expressions created by bit-shift, bit-add, or bit-inversion (e.g. these operations are seen in Figure 3c) of random coefficient sub-expressions (e.g. Figure 3a wherein h0-h2 are coefficients of the FIR filter) out of the digital filter coefficients, thereafter shifting the digital samples

by the number of bits corresponding to the common sub-expression and the virtual common sub-expression, adding (e.g. all the addition boxes in Figure 3c) up all the digital samples shifted by the number of bits corresponding to the common sub-expressions to obtain a composite output value of a common coefficient tap line; obtaining composite output values of random coefficient tap lines by adding up (e.g. y0-y2) the digital samples shifted by the number of bits corresponding to the virtual common sub-expression and the composite output value of the common coefficient tap line being used as a common input; and performing in order delaying (e.g. Figure 3a wherein z^{-1} is the delay for proper FIR fitler) and adding to create filter output values by subsequent compositions of the composite output values of the common coefficient tap Lines and the composite output values of the random coefficient tap lines.

Re claim 8, Pasko et al. further disclose in Figures 2-3 the number of the tap Lines is set as 73 in case where the digital filter is used in a middle frequency terminal of a mobile radio communication system (e.g. page 101 last line of left column and first line of the right column).

Re claim 9, Pasko et al. further disclose in Figures 2-3 the number of bits of the CDS code word is 24 bits (e.g. page 101 last line of left column and first line of the right column).

Re claim 10, Pasko et al. disclose in Figures 2-a digital filter, comprising: a shift register group (e.g. >>3 and >>2 in Figure 3c) including first shift register members each receiving digital samples of k bits as input signals and shifting the received digital samples by bit shift values of filter coefficients that are defined as common sub-

expressions out of filter coefficients that are expressed as code words of n bits within CSD code, and second shift register members shifting code words of the other filter coefficients that are not defined as the common sub-expressions by using the code words of the common sub-expressions not originally common to any filter coefficients, a adder group (e.g. all addition boxes in Figure 3c) including first composite members adding up the shifted digital samples that are output from the first shift register members to provide them to common tap Lines, and second composite members for adding the shifted digital samples that are output from the second shift register members to the composite outputs of the common tap Lines to provide the results to each of corresponding tap Lines; a delay group (e.g. all z^{-1} in Figure 3a) including a plurality of delayers connected to the tap Lines and being connected in series from one another to provide delay to the composite outputs; and an output adder (e.g. last adder in Figure 3a) group including a plurality of adders for adding up the outputs of the delayers and the composite outputs of the tap Lines to create digital output signals of k bit(s).

Re claim 11, it has same limitations cited in claim 10. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 12, Pasko et al. further disclose in Figures 2-3 the common tap Line is a tap Line of filter coefficients having the greatest number of common coefficient sub-expressions out of the filter coefficients (e.g. page 102 right column lines 1-10).

Re claim 13, Pasko et al. further disclose in Figures 2-3 the digital filter is designed with software by a digital signal processor performing shifting, adding, and delaying (e.g. page 100 left column first paragraph under the introduction section and all

the section under page 102 right column including pattern identification, pattern selection, and searching algorithm).

Re claim 14, it is a method claim of claim 1. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 15, Pasko et al. further disclose in Figures 2-3 at least the second sub-expression is formed from the virtual common sub-expression through at least one of a bit-shift, a bit-add and a bit-inversion (e.g. Figure 3b).

Re claim 16, it is a method claim of claim 5. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 17, it is a program storage device claim of claim 1. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 18, it is a system claim of claim 1. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 19, Pasko et al. disclose in Figures 2-3 at least one shift register (e.g. >>3 and >>2 in Figure 3c) for receiving digital samples of input signals and shifting the received digital samples by bit-shift values of filter coefficients that are defined relative to a virtual common sub-expression not originally common to any filter coefficients; a first adder (e.g. first adder that add x and -x>>3 in Figure 3c) for adding shifted digital samples that are output from the at least one shift register to drive a common tap Line; a second adder (e.g. adder for yielding y1 in Figure 3c) for adding shifted digital samples that are output from the at Least one shift register to the output of the common tap line to

drive a tap line corresponding to a filter coefficient; and at Least one delay unit (e.g. z^{-1} in Figure 3a) connected to a tap Line for delaying an output signal component.

Re claim 20, it has same limitations cited claim 19. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 19.

Re claim 21, it is a program storage device claim of claim 20. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 20

Response to Arguments

5. Applicant's arguments filed 05/18/2006 have been fully considered but they are not persuasive.

a. The applicant argues in pages 12-13 for all claims under 102 rejection that the cited reference by Pasko et al. fails to disclose a limitation a virtual common subexpression not originally common to any filter coefficients as cited in the claimed invention.

The examiner respectfully submits that the cited reference clearly discloses the amended limitations "a virtual common subexpression not originally common to any filter coefficients" based on the following reasons: first, the cited reference clearly discloses in the abstract and also in the introduction section that the prior art method is used to optimized the hardware implementation by identifying and eliminating all the common pattern subexpressions in a set of filter coefficients. Second, Figures 1 and 3 clearly support the limitations "a virtual common subexpression not originally common to any filter coefficients" wherein in the

Figure 1c is not common to any of coefficients in Figure 1a-b, nor further in Figure 3c. Third, Figure 2 clearly disclose an overall architecture of achieving the optimized design wherein the coefficients are converted into CSD coefficients and further optimized by the CSD optimization process which eliminated the common subexpression, in another words no subexpression in the designed is repeated as seen in Figures 1c and 3c. Therefore, each set of coefficients will have a unique optimized set of CSE.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

July 17, 2006

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